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10ES33

Third Semester B.E. Degree Examination, June/July 2016
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the following canonical form :

i) $F(x,y,z) = x + \bar{x}y + \bar{x}\bar{z}$

ii) $F(x,y,z) = (x+z)(\bar{x}+y)(y+z)$ **(10 Marks)**

b. Find the minimal POS expression of incompletely specified Boolean function using K–map,

$f(a, b, c, d) = \pi M(1, 2, 3, 4, 9, 10) + \pi d(0, 14, 15)$. **(05 Marks)**

c. Find all the minimal SOP expression of
$f(a, b, c, d) = \Sigma(6, 7, 9, 10, 13) + \Sigma d(1, 4, 5, 11, 15)$ using k – map. **(05 Marks)**

2 a. Find all the prime implicants of the function :
$f(a, b, c, d) = \Sigma(7, 9, 12, 13, 14, 15) + \Sigma d(4, 11)$ using Quine – MaClusky's algorithm. **(10 Marks)**

b. For a given incomplete Boolean function, find a minimal sum and minimal product expression using MEV technique taking least significant bit as map entered variable.
$f(a, b, c, d) = \Sigma(1, 5, 6, 7, 9, 11, 12, 13) + \Sigma d(0, 3, 4)$. **(10 Marks)**

3 a. Implement the function using active low output dual 2 : 4 line decoder IC74139
i) $f_1(A, B, C) = \Sigma m(0, 1, 2, 5)$
ii) $f_2(A, B, C) = \pi M(1, 3, 4, 7)$. **(10 Marks)**

b. Design priority encoder with three inputs, with middle bit at highest priority encoding to 10, most significant bit at next priority encoding to 11 and least significant at least priority encoding 01. **(10 Marks)**

4 a. Define multiplexer and demulitplexer and draw block diagram. **(04 Marks)**

b. Design 4 : 1 multiplexer, draw the circuit using gates. **(06 Marks)**

c. Explain how will you implement the following function using implementation table,
$F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 7, 10, 12, 14)$ with A, B, C as select lines. **(10 Marks)**

PART – B

5 a. Design full adder and draw the circuit using two input NAND gates. **(07 Marks)**

b. Design and draw the circuit of look ahead carry generator using gates. Draw the block diagram of 4–bit parallel adder using look ahead carry generator. **(10 Marks)**

c. Design single bit magnitude comparator and draw the circuit. **(03 Marks)**

6 a. Obtain the following for SR flip–flop :
i) Characteristic equation
ii) Excitation table
iii) State diagram. **(06 Marks)**

b. With the help of a schematic diagram, explain how a serial shift register can be transformed into a i) ring counter ii) Johnson counter. **(04 Marks)**

c. Design mod6 synchronous counter using D–flip–flops. **(10 Marks)**

7 a. A sequential network has one input and one output the state diagram is shown in Fig. Q7(a). Design the sequential circuit using T flip-flops. **(10 Marks)**

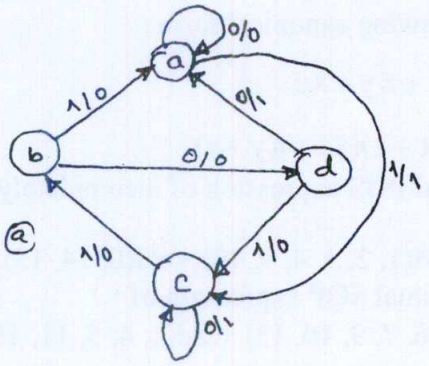

Fig. Q7(a)

b. Derive the transition equations, transition table, state table and state diagram for the following. **(10 Marks)**

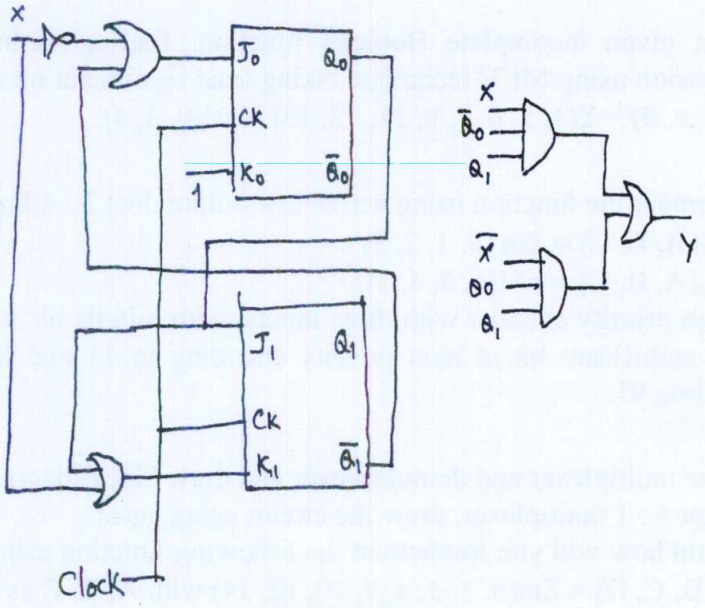

Fig. Q7(b)

8 Write notes on :
a. Mealy and Moore model
b. State machine notation. **(20 Marks)**

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